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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,464	KAWANAKA, SHIGERU	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 9-14* is/are rejected.

7)☒ Claim(s) *3-8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *20020215* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-15 in the paper received on July 28, 2003 is acknowledged.

2. Claims 16-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the paper received on July 28, 2003.

Specification

3. The disclosure is objected to because of the following informalities: on p. 10, lines 32, the specification incorrectly states that "pMOSFET" is a type of substrate.

Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 15 is objected to because of the following informalities: the examiner believes that the word "effected" should be *affected*. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for an insulating film and a semiconductor layer on a semiconductor substrate, does not reasonably provide enablement for an insulating film and a semiconductor layer on an insulating substrate. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

8. The examiner is unable to find any discussion of an insulating film and a semiconductor layer formed on an insulating substrate. SOS (silicon on sapphire) is discussed (p.15, line 32); however this is a silicon film formed directly on a sapphire substrate with no additional insulating film. Furthermore an insulating film is not a semiconductor layer. Therefore the examiner is unable to determine the metes and bounds of claim 11.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 12 recites the limitation "said element isolation region" in the second line. There is insufficient antecedent basis for this limitation in the claim.

12. The examiner believes that claim 12 was intended to claim dependency from claim 9 and not claim 1. The examiner has interpreted claim 12 in this manner.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435).

15. In reference to claim 1, Hazama et al. (USPN 5,162,880, hereinafter referred to as the "Hazama" reference) discloses a similar device. Figures 11a, 11b and 13 illustrate a semiconductor memory device with a memory cell formed of two transistors on a semiconductor layer. The first and second memory transistors are connected in series with one side connected to a bitline and the other side being supplied with a reference potential. Hazama does not disclose forming the transistors on an SOI substrate (a semiconductor layer formed on an insulating film). However the use of an SOI substrate is well known in the art. Venkatasen et al. (USPN 5,736,435, hereinafter referred to as the "Venkatasen" reference) discloses that transistors formed on SOI substrates have the advantage of better performance at lower operating voltages than

those formed on bulk substrates (column 1, lines 30-38). In view of Venkatasen, it would therefore be obvious to implement the device of Hazama onto an SOI substrate.

16. With regard to claim 10, the SOI substrate which Venkatesan discusses is an insulating film and a semiconductor formed on a semiconductor substrate (column 1, lines 41-43).

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435) as applied to claim 1 above and further in view of Yu (USPN 6,534,373 B1).

18. In reference to claim 2, neither Hazama nor Venkatasen discloses implementing partially depleted transistors in the memory cell. However, the use of partially depleted transistors is well known in the art. Yu (USPN 6,534,373 B1) discloses that implementing a partially depleted transistor (such as the device of figure 1) provides the advantages of reduced source-drain junction capacitance and is latch-up free (column 2, lines 1-4). It would therefore be obvious to implement the partially depleted transistors in the memory cell.

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435) and further in view of Yasaitis (USPN 4,722,910) and further in view of Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12-13).

20. In reference to claim 9, Hazama does not disclose surrounding the transistors with an element isolation region. However the use of element isolation regions is well known in the art. Yasaitis discloses that it is customary for active regions to be

surrounded by element isolation region such as field oxides (column 1, lines 14-18). Furthermore Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12) discloses that isolation is critical in the implementation of silicon integrated circuits. The isolation provides devices with the advantages of lower reverse-bias junction leakages and higher breakdown voltages. In view of Yasaitis and Wolf, it would therefore be obvious to surround the memory cell with an element isolating region.

21. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435) and further in view of Yasaitis (USPN 4,722,910) and further in view of Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12-13) and further in view of Cooperman et al. (USPN 5,494,857).

22. So far as understood in claim 12, Hazama does not disclose surrounding the transistors with a trench-type element isolation region. However the use of element isolation regions is well known in the art. Yasaitis discloses that it is customary for active regions to be surrounded by element isolation region such as field oxides (column 1, lines 14-18). Furthermore Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12) discloses that isolation is critical in the implementation of silicon integrated circuits. The isolation provides devices with the advantages of lower reverse-bias junction leakages and higher breakdown voltages. In addition, Cooperman (USPN 5,494,857, hereinafter referred to as the "Cooperman" reference) states that trench-type isolation provides the advantages of higher density, improved isolation, and a higher degree of planarity (column 1, lines 40-46). In view of Yasaitis, Wolf, and

Cooperman, it would therefore be obvious to surround the memory cell with a trench-type element isolating region.

23. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435).

24. In reference to claim 1, Hazama et al. (USPN 5,162,880, hereinafter referred to as the "Hazama" reference) discloses a similar device. Figures 11a, 11b and 13 illustrate a semiconductor memory device with a memory cell formed of two transistors on a semiconductor layer. The first and second memory transistors are connected in series with one side connected to a bitline and the other side being supplied with a reference potential. The threshold value of the transistors is controlled by controlling injection or discharge of an electric charge to or from a body region of one the transistors of a selected memory cell in order to store data (column 10, lines 20-32). Hazama does not disclose forming the transistors on an SOI substrate (a semiconductor layer formed on an insulating film). However the use of an SOI substrate is well known in the art. Venkatasen et al. (USPN 5,736,435, hereinafter referred to as the "Venkatasen" reference) discloses that transistors formed on SOI substrates have the advantage of better performance at lower operating voltages than those formed on bulk substrates (column 1, lines 30-38). In view of Venkatasen, it would therefore be obvious to implement the device of Hazama onto an SOI substrate.

25. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al. (USPN 5,162,880) in view of Venkatasen et al. (USPN 5,736,435) as applied to claim 13 above and further in view of Yu (USPN 6,534,373 B1).

26. In reference to claim 14, neither Hazama nor Venkatasen discloses implementing partially depleted transistors in the memory cell. However, the use of partially depleted transistors is well known in the art. Yu (USPN 6,534,373 B1) discloses that implementing a partially depleted transistor (such as the device of figure 1) provides the advantages of reduced source-drain junction capacitance and is latch-up free (column 2, lines 1-4). It would therefore be obvious to implement the partially depleted transistors in the memory cell.

Allowable Subject Matter

27. Claims 3-8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor memory device which uses a cell made up of two partially depleted SOI transistors of the same conductivity type wherein one of the transistors has its gate coupled to a wordline while the other transistor has its gate coupled to the inverse of the wordline.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ